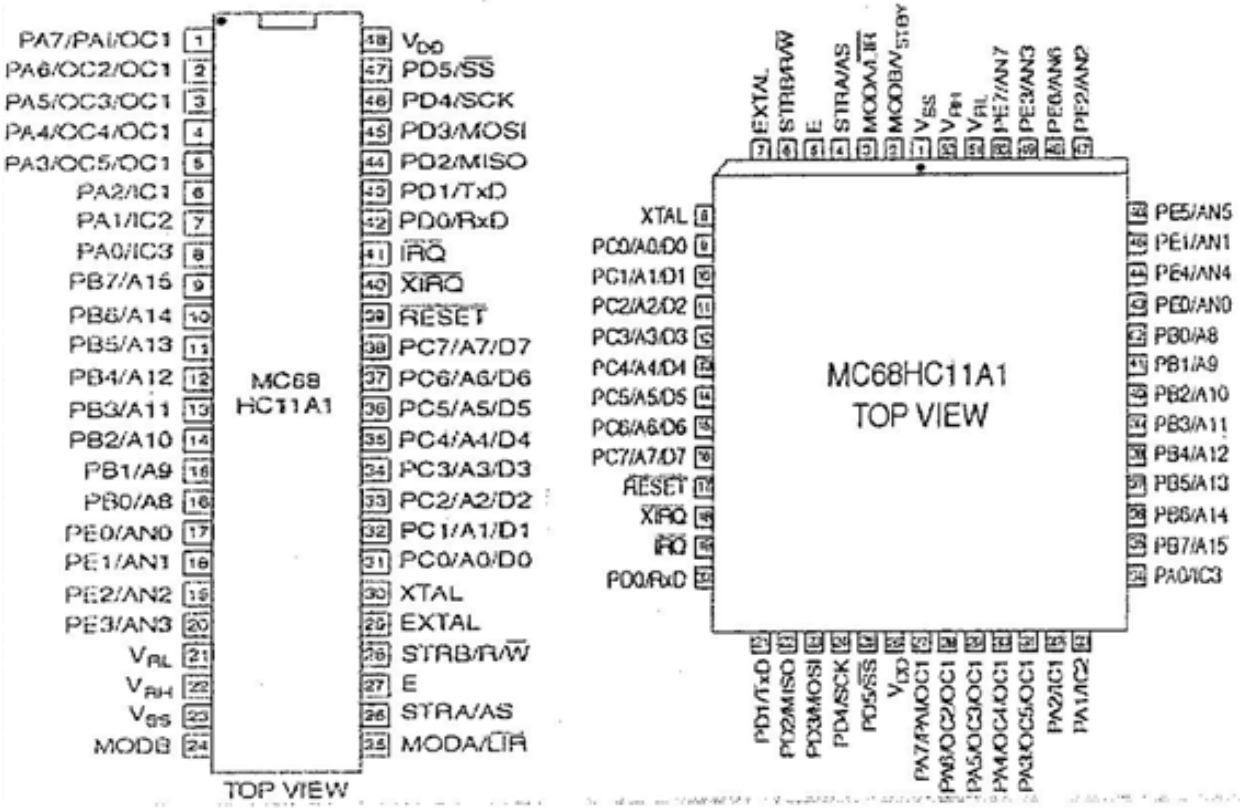
5 System design based on M68HC11

5.1 Pin explanation (DIP48)



VDD (pin 48): Supply voltage towards 68HC11, 5V

VSS (pin 23): Earth (O V) supply voltage to 68HC11

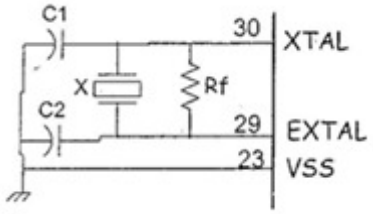
EXTAL (pin 29): XTAL & EXTAL, both used as crystal connector for triggering the oscillator on 68 HC11 chip.

XTAL (pin 30): Oscillator circuit:

$C_1 = C_2 = 20\ pF \mp 10pF$

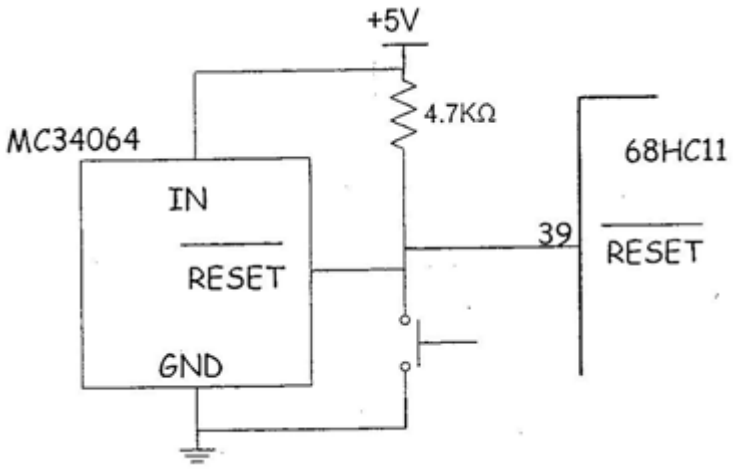
X = 8 MHz normally

Rf = 1 MΩ - 20MΩ



E (pin 27): Output clock signal E which operates at a frequency of ¼ XTAL frequency (E = 2MHz when XTAL = 8 MHz). It been used as reference signal in the other bus signal timing. And it should be used in address decoding circuit.

RESET (pin 39): 68HC11 will be reset when RESET pin is at logic '0' for at least eight signal cycle E (2 μ s for XTAL 8 MHz) when oscillator is operating. Motorola recommend using MCM34064 in the reset circuit:

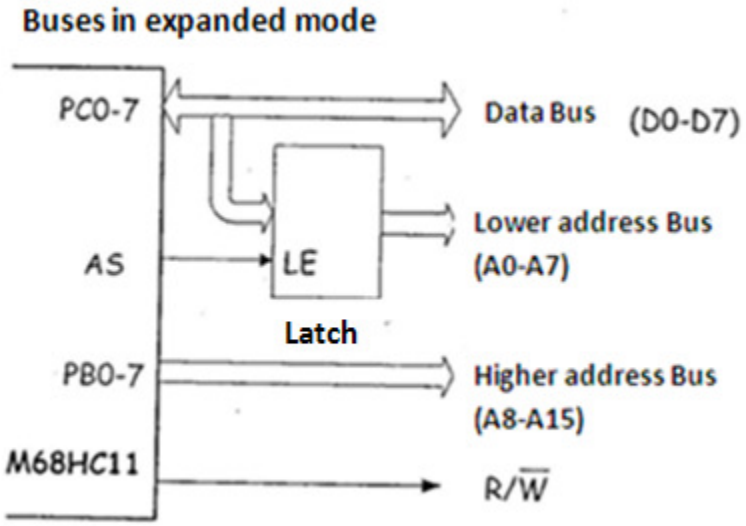


MODB (pin 24): MODA & MODB used to set as the operating modes for 68HC11.

MODA (pin 25): Voltage level at MODA & MODB pin will latch when the rising of edge signal RESET. This logic level will determine which 68HC11 will operate as below:

Input Logic		Operating Mode
MODB	MODA	
1	0	Single Chip
1	1	Expanded
0	0	Special Bootstrap
0	1	Special Test

PCO-PC7/AD0 – AD7 (31 - 38):	Input-output port is two ways in 8 bit mode single chip and bootstrap. Also act as address bus/multiplexed data in widest mode. When AS logic '1', PC0-7 became the lower bus address (A0-A7). While AS logic at '0', PC0-7 became two ways data bus (D0-D7).
STRA/AS (pin 26):	These expanded signal mode acts as a clock for locking the lower outer address (A0-A7) from address bus/multiplexed data PC0-7. Usually, it connected to the lock variable for lock type 74x373@74x573. In the single chip/bootstrap mode, it will become handshake signal transfers data via port C.
STRB/W (pin 28):	It is expanded mode signal that functioning as readable variable signal (when high) and writable variable (when low) for memory and outside I/O. while mode of single chip/bootstrap will became handshake signal transfer through port C.
PB7-PB0/A15-A8 (9-16):	8 bit Output port in mode of single chip and bootstrap. And act as higher address bus (A8-A15) in expanded mode.



PA.7-0 (pin 1-8): Port input-output A consists of only 3 pin input (PA.0-PA.2), only 4 pin output (PA.3-PA.6) & 1 two ways pin (PA.7). Below is the alternative function for Port A:

Bit	Alternate Function
PA.0-PA.2	Input capture
PA.3-PA.6	Output compare
PA.7	I/O general purpose @ pulse accumulator input @ output pin for checklist timer 1

PD0-PD5 (42-47): 6 bit two ways input/output port, also functioning as serial communication port with below alternate function:

Bit	Alternate Function	
PD.0	RXD-input for serial port	Serial communication interface
PD.1	TXD-output for serial port	
PD.2	MISO	Serial peripheral interface
PD.3	MOSI	
PD.4	SCK	
PD.5	SS	

PE0-PE3 (p 17-20): AN0-AN3 — Input port for general purpose E. And as input for internal analog converter to digital 68HC11. Note: 68HC11 with 52 pin have 8 bit port E (8 input A/D converter)

V_{RH} (pin 22): V_{RL} (pin 21) — Give the reference voltage for the internal A/D converter. Usually, V_{RH} is connected to VDD & V_{RL} to VSS

$\overline{XIRQ}$ (pin 40): $\overline{IRQ}$ (pin 41) — Interrupt input for 68HC11.
XIRQ (NMI) – interrupt cannot be masked
IRQ – interrupt can be masked

5.2 Internal operation when reset

1. Registers and control bits of internal peripheral start with original value (default).
   > Internal RAM is activated at address $00-$FF
   > Control register of internal peripheral located at address $1000-$103F
   > Port B & C become the address bus and data for the widest mode
   > Port B & C become the I/O port in the single chip/bootstrap mode
   > Port A (0, 1, 2, 7), D & E become high input impedance
   > Port A3-A6 become output while disabled the interrupt
   > Counter timer set to $0000. While A/D converter s uncertainty
   > Serial communication interface is uncertainty
   > Serial peripheral interface is disabled

2. SP contents and other CPU registers are uncertainty.

3. CPU will achieved the reset vector at address $FFFE, $FFFF for the single chip and expanded mode while address $BFFE, $BFFF are for the bootstrap mode. 68HC11 will implement the Instructions that starts from given by contents $FFFE, $FFFF @ $BFFE, $BFFF.

Widest mode @ single chip	Bootstrap mode
Start : org $E000	Start: org $B600 ; E^2PROM
ldx #name	ldx #name
ldaa 0,x	ldaa 0, x
beq end	beq end
jsr show	jsr show
inx	inx
bra start	bra start
Name: fcb 'rosbi', 0	Name: fcb 'rosbi', 0
:	:
; reset vector	; reset vector
Org $FFFE	org $BFFE
fdb start	fdb start

Vector – Address pointing to the beginning of a program that would treat a situation like reset and interrupt.

Content of vector = address initial treatment program.

5.3 Operating mode of 68HC11

a) Single chip modes

In this mode, 68HC11 needs no bus data/output address for handling. So, port B and C can be used as general purpose I/O . Only the internal memory will be used. The program must be written in the internal ROM at $E000-$FFFF address. Motorola services is needed for the ROM program and useful for internal ROM 68HC11.

b) Widest mode

For 68HC11, it need the data bus/output address for handling. Thus, port B and C are used as data bus and output address. In this mode, the space of maximum address that can be reached is 64K. And very beneficial for system that will spent on the bigger I/O memory.

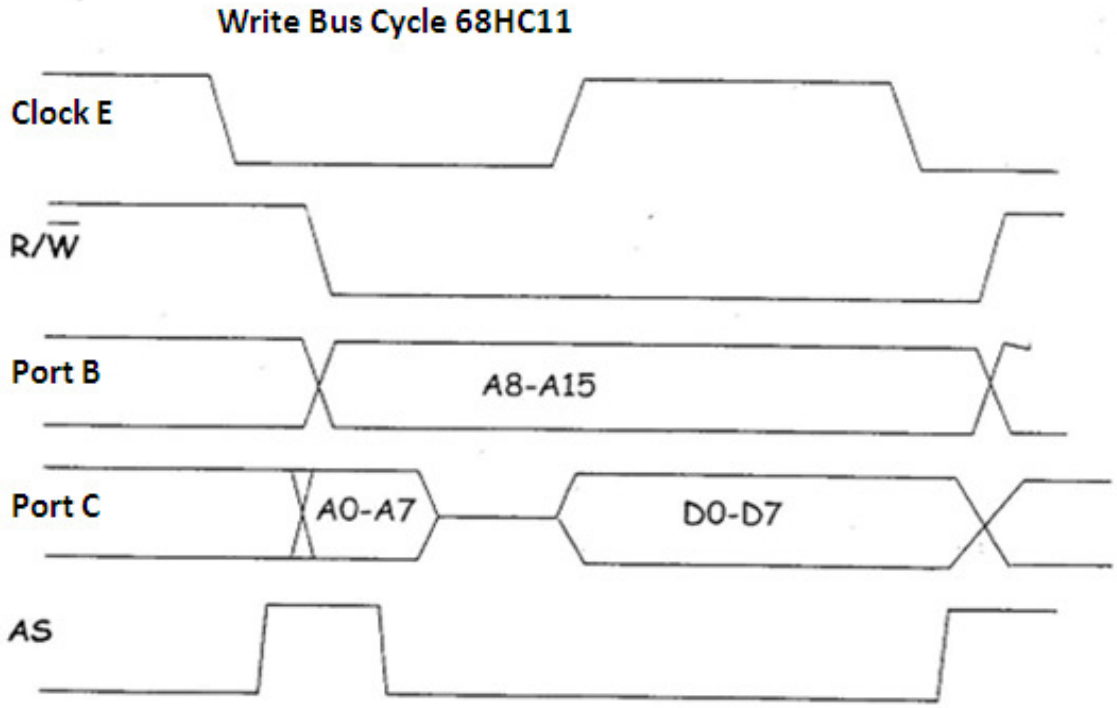
c) Bootstrap mode

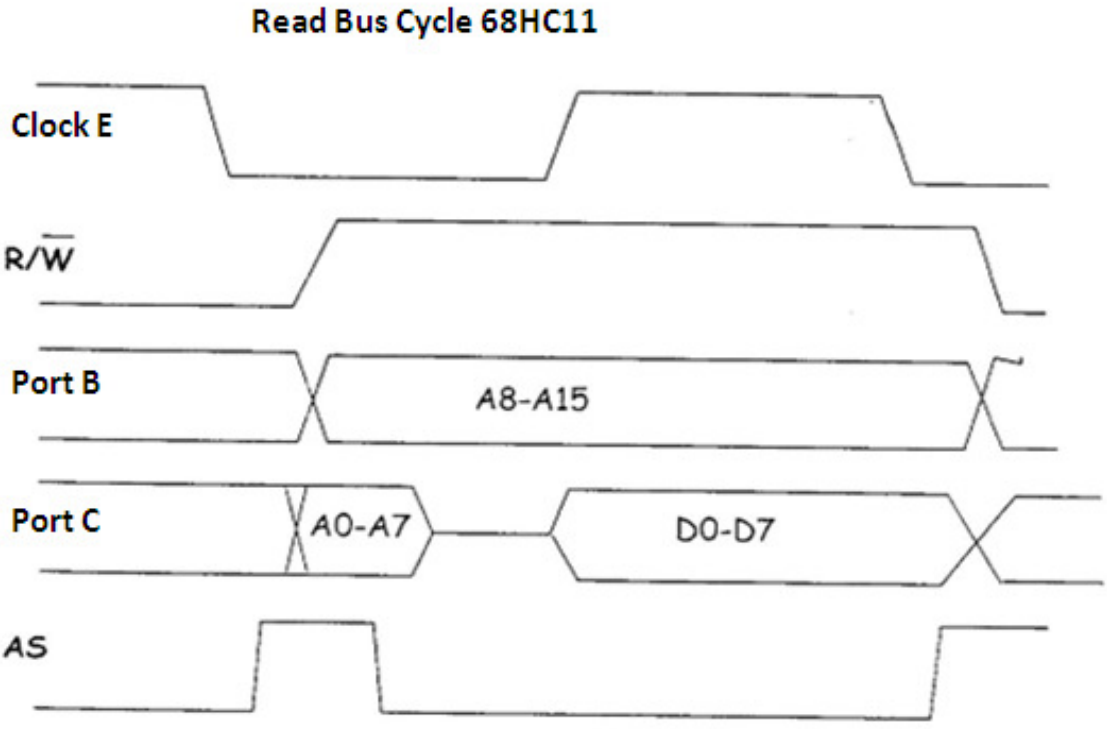
When handling this mode, the special internal ROM ($BF00-$BFFF) called as Bootstrap ROM will be activated. The reset vector will accomplished from this ROM and a program (bootstrap program) in this ROM that written as MOTOROLA will carry out. The bootstrap program is responsible on reading the 256 byte machine code from serial communication medium, and store it inside the internal RAM ($00-$FF) and carry out the machine code starting from address $00.
In this mode too, the data bus/output address is unnecessary for handling. Therefore, port B and C can be used as general purpose I/O and useful for the internal E^2PROM learning and programming.

d) Test mode

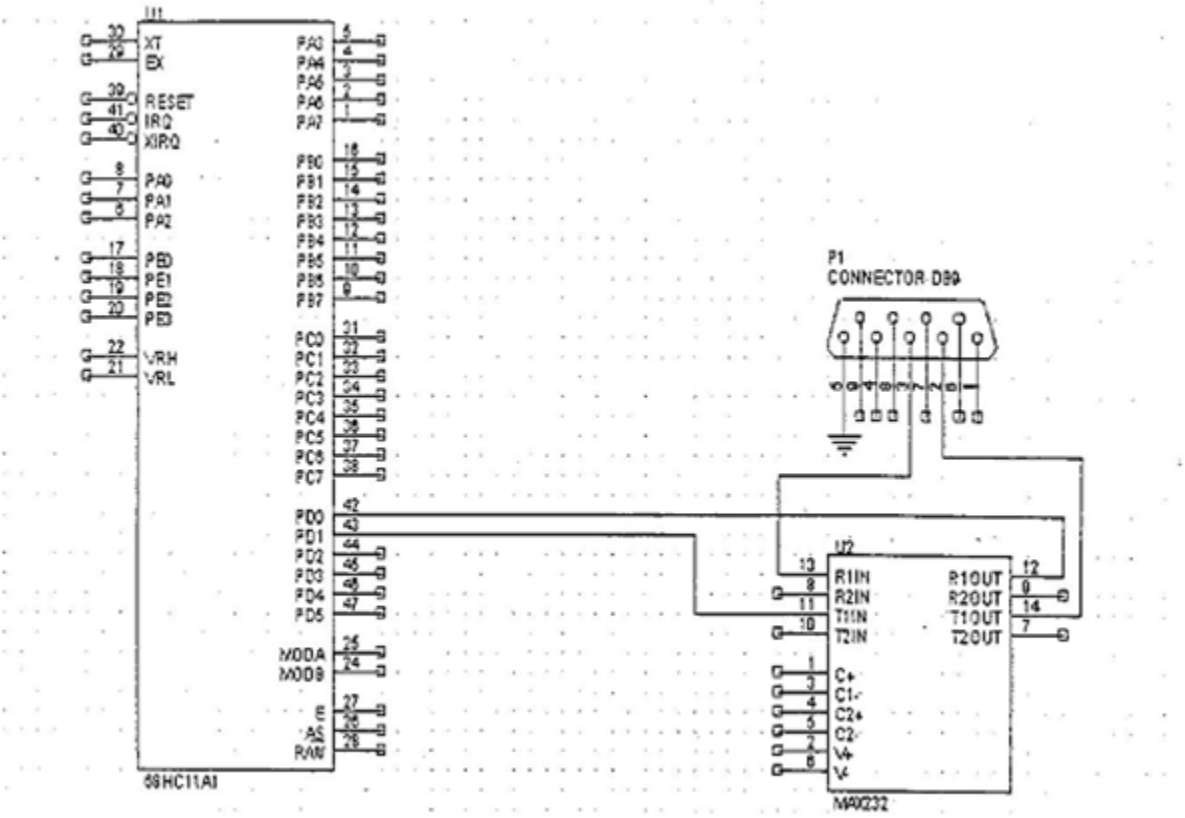
Used by the MOTOROLA for work of internal testing.

5.4 Timing diagram of 68HC11 in widest mode



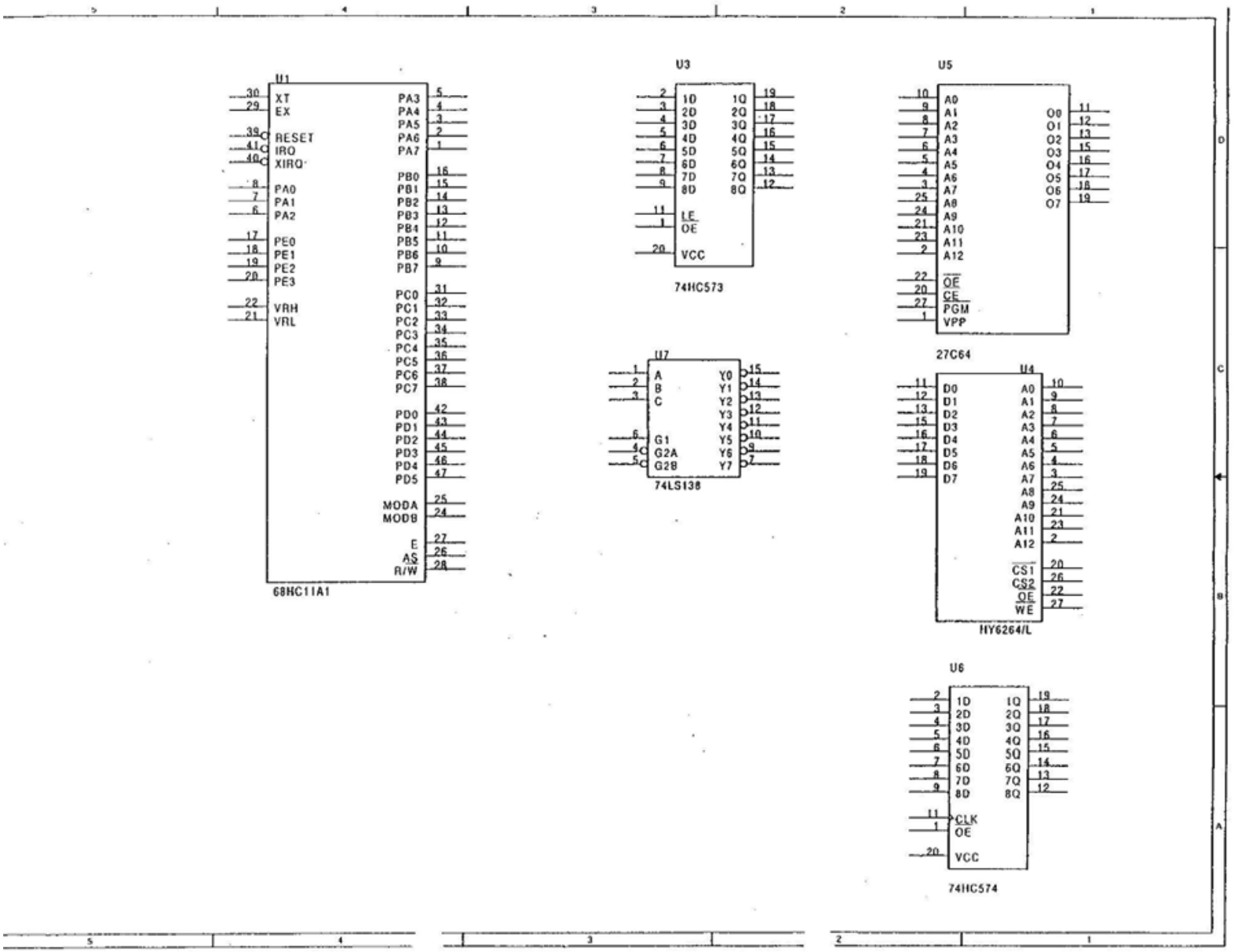


5.5 Micro Controller Circuit 68HC11 in Bootstrap mode

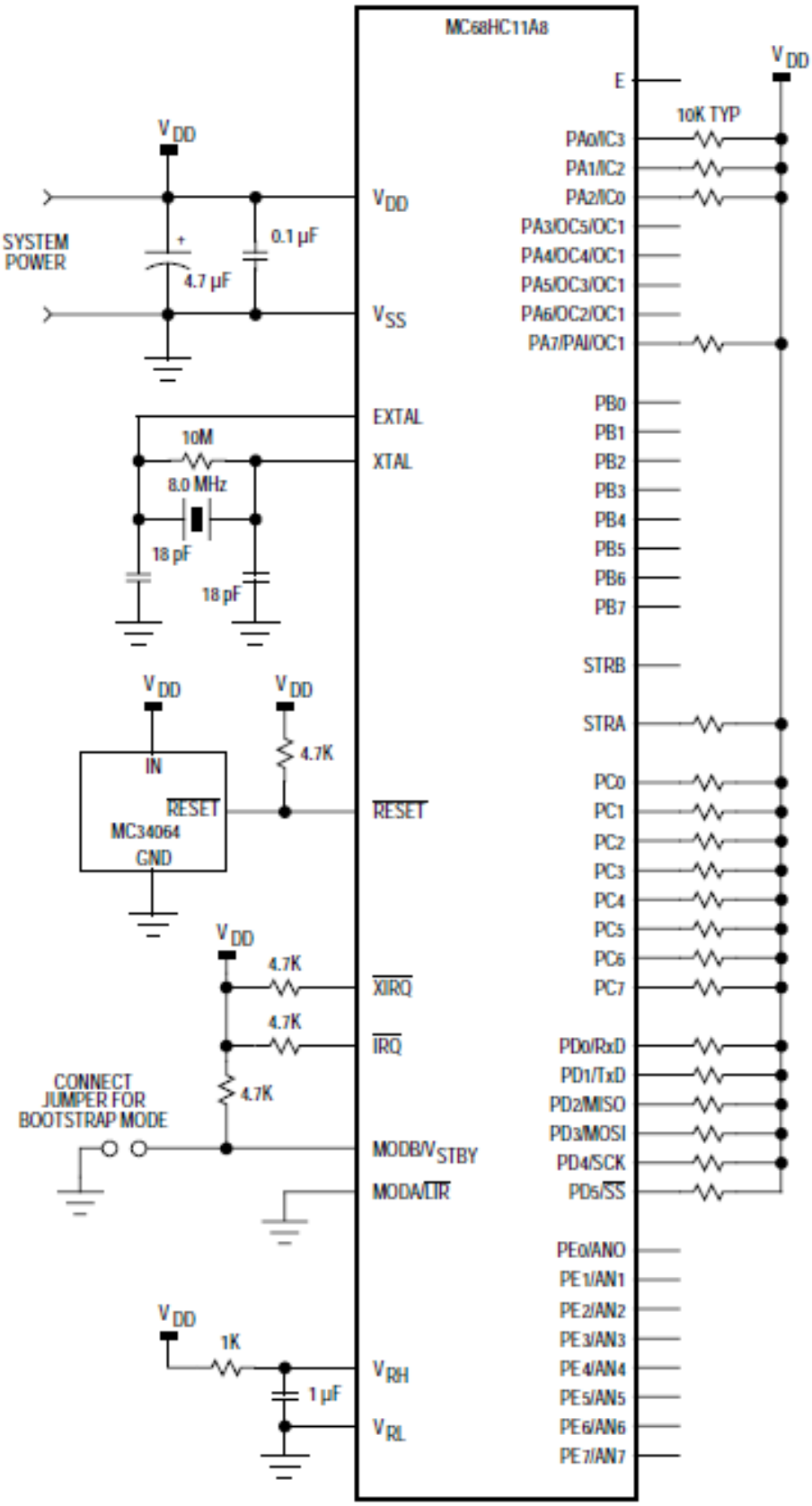


5.6 Micro Controller 68HC11 in expanded mode

Refer to schematic!


U1
XT
EX
RESET
IRQ
XIRQ
PA0
PA1
PA2
PE0
PE1
PE2
PE3
VRH
VRL
PA3
PA4
PA5
PA6
PA7
PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7
PC0
PC1
PC2
PC3
PC4
PC5
PC6
PC7
PD0
PD1
PD2
PD3
PD4
PD5
MODA
MODB
E
AS
R/W
68HC11A1
U3
1D
2D
3D
4D
5D
6D
7D
8D
LE
OE
VCC
1Q
2Q
3Q
4Q
5Q
6Q
7Q
8Q
74HC573
U5
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
OE
CE
PGM
VPP
O0
O1
O2
O3
O4
O5
O6
O7
27C64
U7
A
B
C
G1
G2A
G2B
Y0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
74LS138
U4
D0
D1
D2
D3
D4
D5
D6
D7
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
CS1
CS2
OE
WE
HY6264/L
U6
1D
2D
3D
4D
5D
6D
7D
8D
CLK
OE
VCC
1Q
2Q
3Q
4Q
5Q
6Q
7Q
8Q
74HC574

Single chip-mode



Expanded mode

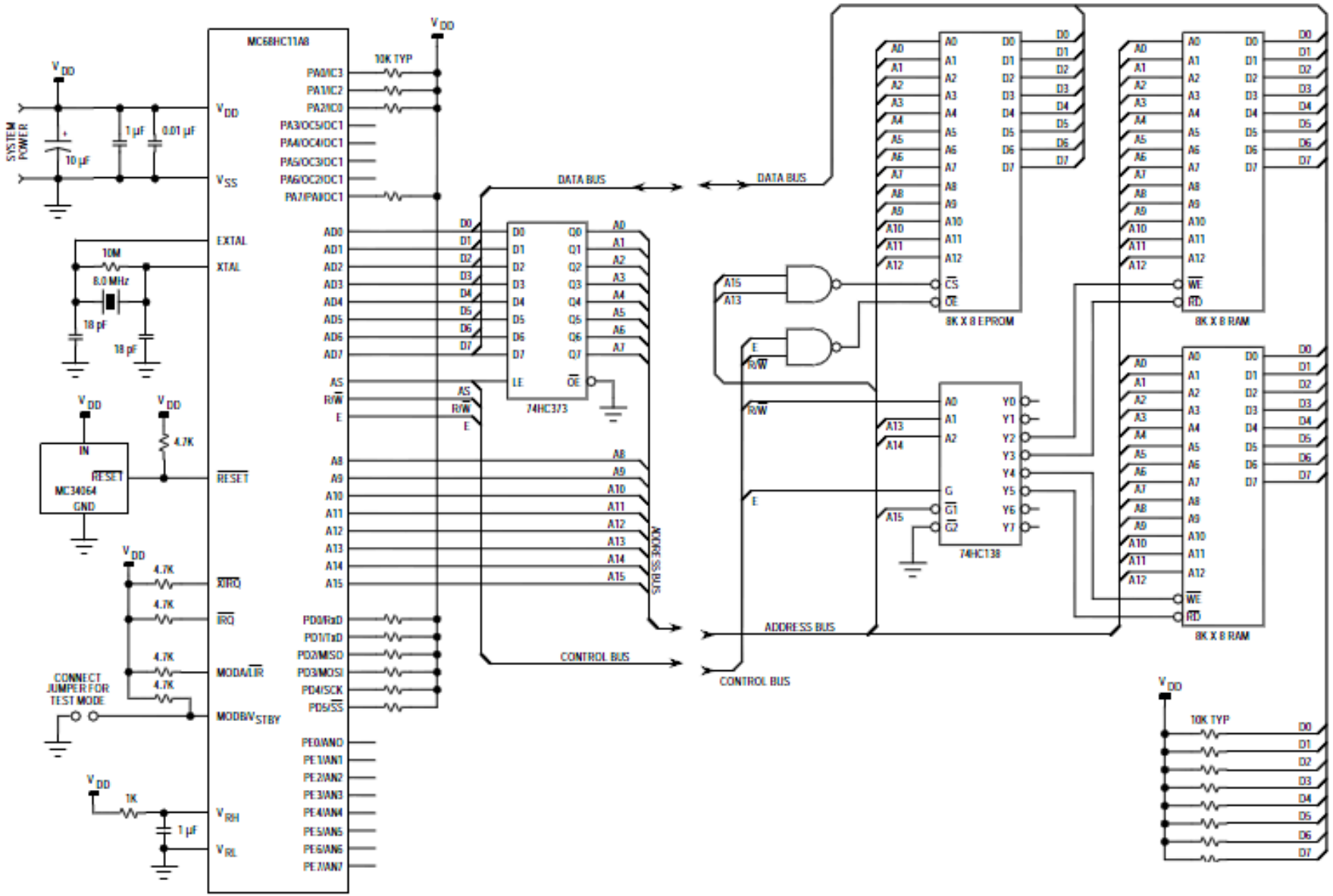


Table 3 MC68HC11A8 Register and Control Bit Assignments (Sheet 1 of 2)

(The register block can be remapped to any 4K boundary.)

	Bit 7	6	5	4	3	2	1	Bit 0	
$1000	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	PORTA
$1001									Reserved
$1002	STAF	STAI	CWOM	HNDS	OIN	PLS	EGA	INVB	PIOC
$1003	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	PORTC
$1004	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	PORTB
$1005	PCL7	PCL6	PCL5	PCL4	PCL3	PCL2	PCL1	PCL0	PORTCL
$1006									Reserved
$1007	DDC7	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0	DDRC
$1008	0	0	PD5	PD4	PD3	PD2	PD1	PD0	PORTD
$1009	0	0	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	DDRD
$100A	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0	PORTE
$100B	FOC1	FOC2	FOC3	FOC4	FOC5	0	0	0	CFORC
$100C	OC1M7	OC1M6	OC1M5	OC1M4	OC1M3	0	0	0	OC1M
$100D	OC1D7	OC1D6	OC1D5	OC1D4	OC1D3	0	0	0	OC1D
$100E	Bit 15	14	13	12	11	10	9	Bit 8	TCNT (High)
$100F	Bit 7	6	5	4	3	2	1	Bit 0	TCNT (Low)
$1010	Bit 15	14	13	12	11	10	9	Bit 8	TIC1 (High)
$1011	Bit 7	6	5	4	3	2	1	Bit 0	TIC1 (Low)
$1012	Bit 15	14	13	12	11	10	9	Bit 8	TIC2 (High)
$1013	Bit 7	6	5	4	3	2	1	Bit 0	TIC2 (Low)
$1014	Bit 15	14	13	12	11	10	9	Bit 8	TIC3 (High)
$1015	Bit 7	6	5	4	3	2	1	Bit 0	TIC3 (Low)
$1016	Bit 15	14	13	12	11	10	9	Bit 8	TOC1(High)
$1017	Bit 7	6	5	4	3	2	1	Bit 0	TOC1 (Low)
$1018	Bit 15	14	13	12	11	10	9	Bit 8	TOC2 (High)
$1019	Bit 7	6	5	4	3	2	1	Bit 0	TOC2 (Low)
$101A	Bit 15	14	13	12	11	10	9	Bit 8	TOC3 (High)
$101B	Bit 7	6	5	4	3	2	1	Bit 0	TOC3 (Low)
$101C	Bit 15	14	13	12	11	10	9	Bit 8	TOC4 (High)
$101D	Bit 7	6	5	4	3	2	1	Bit 0	TOC4 (Low)
$101E	Bit 15	14	13	12	11	10	9	Bit 8	TOC5 (High)
$101F	Bit 7	6	5	4	3	2	1	Bit 0	TOC5 (Low)
$1020	OM2	OL2	OM3	OL3	OM4	OL4	OM5	OL5	TCTL1
$1021	0	0	EDG1B	EDG1A	EDG2B	EDG2A	EDG3B	EDG3A	TCTL2
$1022	OC1I	OC2I	OC3I	OC4I	OC5I	IC1I	IC2I	IC3I	TMSK1
$1023	OC1F	OC2F	OC3F	OC4F	OC5F	IC1F	IC2F	IC3F	TFLG1
$1024	TOI	RTII	PAOVI	PAII	0	0	PR1	PR0	TMSK2
$1025	TOF	RTIF	PAOVF	PAIF	0	0	0	0	TFLG2

Table 3 MC68HC11A8 Register and Control Bit Assignments (Sheet 2 of 2)

(The register block can be remapped to any 4K boundary.)

	Bit 7	6	5	4	3	2	1	Bit 0	
$1026	DDRA7	PAEN	PAMOD	PEDGE	0	0	RTR1	RTR0	PACTL
$1027	Bit 7	6	5	4	3	2	1	Bit 0	PACNT
$1028	SPIE	SPE	DWOM	MSTR	CPOL	CPHA	SPR1	SPR0	SPCR
$1029	SPIF	WCOL	0	MODF	0	0	0	0	SPSR
$102A	Bit 7	6	5	4	3	2	1	Bit 0	SPDR
$102B	TCLR	0	SCP1	SCP0	RCKB	SCR2	SCR1	SCR0	BAUD
$102C	R8	T8	0	M	WAKE	0	0	0	SCCR1
$102D	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK	SCCR2
$102E	TDRE	TC	RDRF	IDLE	OR	NF	FE	0	SCSR
$102F	R7/T7	R6/T6	R5/T5	R4/T4	R3/T3	R2/T2	R1/T1	R0/T0	SCDR
$1030	CCF	0	SCAN	MULT	CD	CC	CB	CA	ADCTL
$1031	Bit 7	6	5	4	3	2	1	Bit 0	ADR1
$1032	Bit 7	6	5	4	3	2	1	Bit 0	ADR2
$1033	Bit 7	6	5	4	3	2	1	Bit 0	ADR3
$1034	Bit 7	6	5	4	3	2	1	Bit 0	ADR4
$1035									Reserved
$1038									Reserved
$1039	ADPU	CSEL	IRQE	DLY	CME	0	CR1	CR0	OPTION
$103A	Bit 7	6	5	4	3	2	1	Bit 0	COPRST
$103B	ODD	EVEN	0	BYTE	ROW	ERASE	EELAT	EEPGM	PPROG
$103C	RBOOT	SMOD	MDA	IRV	PSEL3	PSEL2	PSEL1	PSEL0	HPRIO
$103D	RAM3	RAM2	RAM1	RAM0	REG3	REG2	REG1	REG0	INIT
$103E	TILOP	0	OCCR	CBYP	DISR	FCM	FCOP	TCON	TEST1
$103F	0	0	0	0	NOSEC	NOCOP	ROMON	EEON	CONFIG